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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/652,998	08/31/2000	D. Mark Durcan	98-1068.06	4016

7590 07/30/2003

ATTN: RUSSELL D. SLIFER
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MINNEAPOLIS, MN 55458-1009

EXAMINER

MAI, ANH D

ART UNIT	PAPER NUMBER
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2814

DATE MAILED: 07/30/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/652,998

Applicant(s)

DURCAN ET AL.

Examiner

Anh D. Mai

Art Unit

2814

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 05 May 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 13,14,67 and 68 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 13,14,67 and 68 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on May 5, 2003 has been entered.

Status of the Claims

2. Amendment filed May 5, 2003 has been entered as Paper No. 18. Claims 13 and 67 have been amended. Claims 13, 14, 67 and 68 are pending.

Claim Objections

3. Claim 14 is objected to because of the following informalities:

Claim 14 recites: "wherein said top capacitor plate extend toward a top of said contact.

As shown in Fig. 11A, the top capacitor plate 24C only extend toward the contact 36, since plate 24C appears to level off and the specification does not support that the area is the top of the contact.

Appropriate correction is required.

Response to Amendment

4. The amendment filed June 24, 2002 (Paper No. 12) and May 5, 2003 (Paper No. 18) are objected to under 35 U.S.C. 132 because they introduce new matters into the disclosure. 35 U.S.C. 132 states that no amendment shall introduce new matter into the disclosure of the

Art Unit: 2814

invention. The added material which is not supported by the original disclosure is as follows:

“the top capacitor plate includes a lateral clearance opening at the first level around the contact and does not vertically descend between each of the first, second and third bottom capacitor plates” (as recites in claim 13, lines 13-14).

Applicant is required to cancel the new matter in the reply to this Office Action.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 13 and 14 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

There does not appear to be a written description of the claim limitations in the application as filed.

a) the top capacitor plate includes a lateral clearance opening at the first level around the contact and does not vertically descend between each of the first, second and third bottom capacitor plates. (claim 13, lines 13-14).

As shown in Fig. 12, the top capacitor plate 24c lining the trench between the second and third bottom capacitor plates (middle of the drawing). Clearly, the top capacitor plate 24C is vertically descent between the second and third bottom capacitor plates. (See below).

As best understood by the examiner, the top capacitor plate is vertically descent between each of the second and third bottom capacitor plates but does not descent between the first and second bottom capacitor plate.

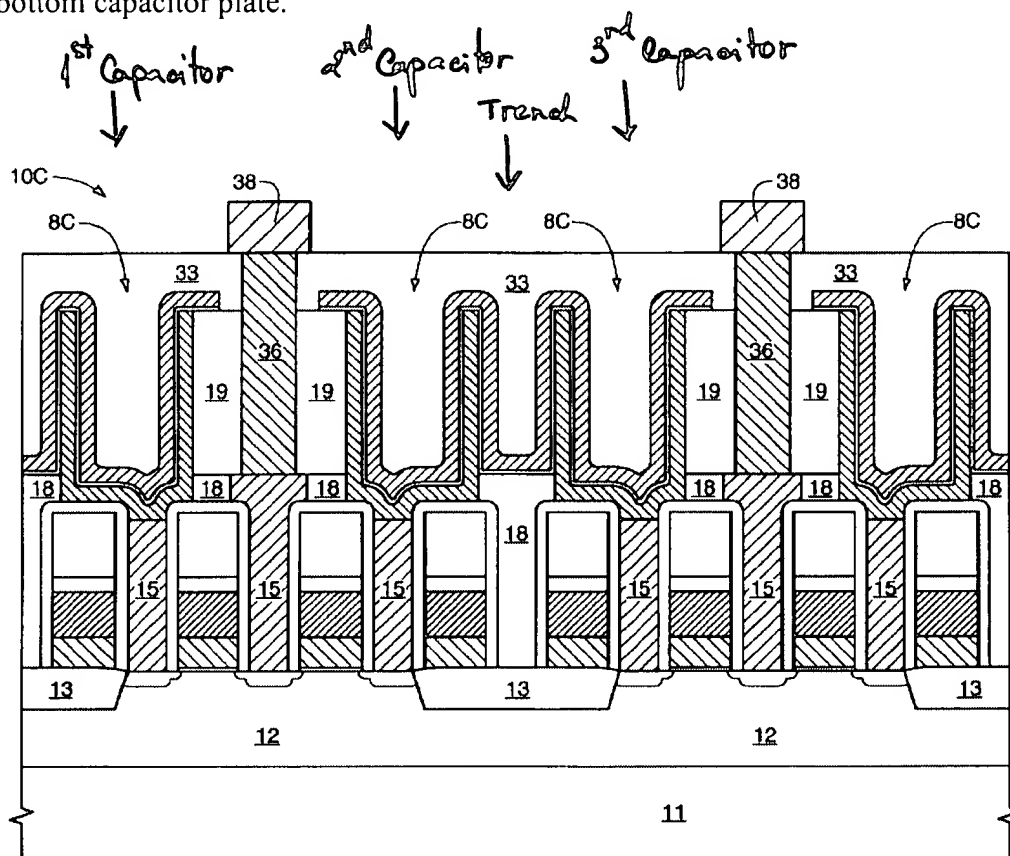


FIG. 12

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 13 and 14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The limitations of claim 13 appears to contradicting each other because:

lines 12-14 recites: “the top capacitor plate includes a lateral clearance opening at the first level around the contact and does not vertically descend between each of the first, second and third bottom capacitor plates and the contact”.

While lines 14-16 recites: “wherein said top capacitor plate lines a side of said trench and further lines a bottom of said trench”.

Note that, the trench is locate between the second the third bottom capacitor plates (lines 8-9). (See Fig. 12 above).

How can top capacitor plate lining the side (vertically descent) of the trench be characterized as does not vertically descent ?

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

7. Claims 13, 14 and 68 are rejected under 35 U.S.C. 103(a) as being unpatentable over Becker (U.S. Patent No. 5,770,498) of record, in view of Applicant admitted prior art.

With respect to claim 13, as best understood by the examiner, Becker teaches an array of capacitors substantially similar as claimed including:

- a first bottom capacitor plate (44);
- a second bottom capacitor plate (44);
- a third bottom capacitor plate (44); (not shown);

Art Unit: 2814

a contact (54) between the first bottom capacitor plate and the second bottom capacitor plate, the contact downwardly extends from a vertical height above a contact area (32B);

a trench between the second bottom capacitor plate (44) and the third bottom capacitor plate (44);

a common top capacitor plate (50) over the first bottom capacitor plate (44), the second bottom capacitor plate (44), and the third bottom capacitor plate (44), wherein the top capacitor plate (50) extends toward the contact (54) at a first level within the array, the top capacitor plate (50) includes a lateral clearance opening at the first level around the contact (54) and vertically descent between each of the first, second and third bottom capacitor plates (44), and wherein the top capacitor plate (50) lines a side of the trench and further lines a bottom of the trench at a second level within the array; and

a dielectric (46) between the top capacitor plate (50) and the first, second, and third bottom capacitor plates (44). (See Fig. 10).

Thus, Becker is shown to teach all the features of the claim with the exception of the top capacitor plate (50) does not vertically descent between the contact.

However, the admitted prior art teaches: the top capacitor plate 24B can be formed not to vertically descent between the contact (5). (See Fig. 3).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the top capacitor plate of Becker not to vertically descent between the contact as taught by the admitted prior art because the portion of the top electrode and the

Art Unit: 2814

dielectric layer to be clear for forming the bit line contact are more accessible. (see page 4, lines 7-11).

With respect to the third bottom capacitor plate (44), although Becker does not show a third bottom capacitor plate (44) in the drawing, however, one having ordinary skill in the art should recognize that the third bottom capacitor plate is actually the first bottom capacitor plate of the adjacent cell, on the outside (left and right) of the first and second bottom capacitor plates (44) since the capacitors of Becker are formed in an array, as shown in Fig. 1 (prior art) of the present invention. (See below).

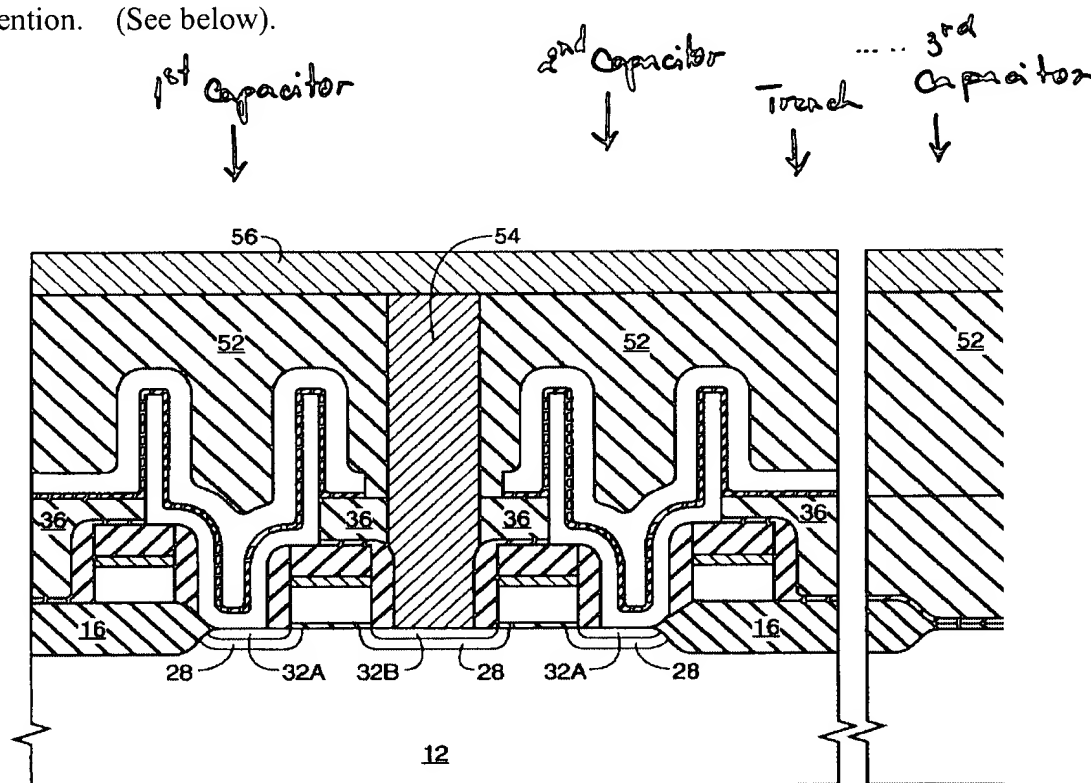


FIG. 10

Art Unit: 2814

With respect to claim 14, as best understood by the examiner, the top capacitor plate (50) extends toward the contact (54).

With respect to claim 67, Becker teaches an array of capacitor substantially as claimed including:

first, second and third memory cell capacitors comprising first, second and third bottom (not shown) container-shaped electrodes (44), respectively;

a bit line contact (54) laterally positioned between the first and second memory cell, the bit line contact (54) downwardly extends from a vertical height above the top of the first and second bottom electrodes (44);

a trench laterally positioned between the second (44) and third (not shown) bottom electrodes; (See Fig. 10);

a common top electrode (50) capacitively coupled to the first, second and third electrodes (44) via a capacitor dielectric layer (46), wherein the top electrode (50) includes a lateral clearance opening around the bit line contact, the top electrode (50) is capacitively coupled to an interior of the first, second and third bottom electrodes (44) and a portion of the exterior of the second and third bottom electrodes (44) located only in the trench; and

a bit line contact insulation region (36/52) surrounding the bit line contact (54) and filling the region between the bit line contact (54) and the bottom electrodes (44). (See Fig. 10).

Art Unit: 2814

Thus, Becker is shown to teach all the features of the claim with the exception of the top electrode (50) is formed to includes an lateral clearance opening above the top of the first bottom electrode.

However, the admitted prior art teaches: the top electrode 24B can be formed to include an opening above the top of the first bottom electrode (20). (See Fig. 3).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the opening of the top electrode (50) above the top of the first bottom electrode (44) of Becker as taught by the admitted prior art because the portion of the top electrode and the dielectric layer to be clear for forming the bit line contact are more accessible. (see page 4, lines 7-11).

With respect to the third bottom container-shaped electrode (44), the same reasoning as that of claim 13 is also applied here.

With respect to claim 68, Becker teaches an array of capacitor substantially as claimed including:

first, second and third memory cell capacitors comprising first, second and third (not shown) bottom container-shaped electrodes (44), respectively;

a bit line contact (54) laterally positioned between the first and second memory cell, the bit line contact downwardly extends from a vertical height above a top of the first and second bottom electrodes (44);

a trench laterally positioned between the second (44) and third bottom electrodes;

a common top electrode (50) capacitively coupled to the first, second and third electrodes (44) via a capacitor dielectric layer (46), wherein the top electrode (50) includes a lateral clearance opening around the bit line contact, the top electrode (50) is capacitively coupled to an interior of the first, second and third bottom electrodes (44) and a portion of the exterior of the second and third bottom electrodes (44) located in the trench; and

a bit line contact insulation region (36/52) surrounding the bit line contact (54) and filling a region between the bit line contact (54) and the first and second bottom electrodes (44). (See Fig. 10).

Thus, Becker is shown to teach all the features of the claim with the exception of the array capacitor is formed such that a bit line contact insulation region prevents the top electrode from downwardly extending between the bit line contact and the first and second bottom electrodes.

However, the admitted prior art teaches forming the bit line contact insulation region (60B) between the first and second bottom electrodes (20) to prevent the top electrode from downwardly extending between the bit line contact and the first and second bottom electrodes. (See Fig. 3).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the bit line contact insulation region of Becker between the first and second bottom electrodes as taught by the admitted prior art because the portion of the top electrode and the dielectric layer to be clear for forming the bit line contact are more accessible. (see page 4, lines 7-11).

Art Unit: 2814

With respect to the third (not shown) bottom container-shaped electrode (44), the same reasoning as that of claim 13 is also applied here.

Response to Arguments

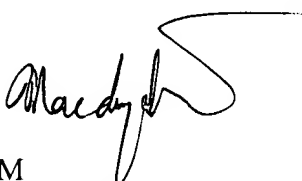
8. Applicant's arguments with respect to all claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh D. Mai whose telephone number is (703) 305-0575. The examiner can normally be reached on 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (703) 306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.


A.M
July 26, 2003